What is claimed is:

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1. A dielectrically separated wafer having a plurality of dielectrically separated silicon islands mutually defined by a dielectrically separating oxide film on the surface of the wafer, wherein said dielectrically separated silicon islands comprise:

a high concentration impurity layer formed on the bottom of the islands; and

a low concentration impurity layer having an identical conductivity laminated on the high concentration impurity layer.

2. A dielectrically separated wafer fabrication process comprising the steps of:

forming a high concentration impurity layer including at high concentration an impurity of identical conductivity at a specified depth range below the surface of the silicon wafer, and a low concentration impurity layer including at low concentration an impurity of identical conductivity at a range deeper than this high concentration impurity layer;

forming dielectrically separating grooves deeper than said high concentration impurity layer on this silicon wafer surface;

forming a dielectrically separating oxide film on each of the surfaces of these dielectrically separating grooves and the silicone wafer;

laminating a polysilicon layer on this dielectrically separating oxide film; and

realizing a plurality of dielectrically separated silicon islands separated by said dielectric separating oxide film on a polished surface by grinding and polishing the silicon wafer from the undersurface; and

wherein said high concentration impurity layer is formed on the bottom of these dielectrically separated silicon islands and said low concentration impurity layer is formed on this high concentration impurity layer.

3. A dielectrically separated wafer having a polysilicon layer and a plurality of polysilicon island mutually separated by a dielectrically separating oxide film formed on the surface of this polysilicon layer, wherein:

said polysilicon layer has a seed polysilicon layer grown by a low temperature CVD method on the interface with said dielectrically separating oxide film.

4. A fabrication method for a dielectrically separated wafer comprising the steps of:

forming dielectrically separating grooves on the surface of the silicon wafer;

forming a dielectrically separating oxide film on the surface of the silicon wafer, including the surfaces of these dielectrically separating grooves;

growing a polysilicon layer on the surface of this dielectrically separating oxide film;

grinding and polishing this silicon wafer form the underside for providing a plurality of dielectrically separated silicon islands separated by the dielectrically separating oxide film on this polished surface;

wherein in growing said polysilicon layer, the method further comprises the steps of;

growing a seed polysilicon layer in advance by the low temperature CVD method on the surface of said dielectrically separating oxide film; and

subsequently, growing said polysilicon layer on the surface of said seed polysilicon layer using the high temperature CVD method.

5. A dielectrically separated wafer, having a plurality of dielectrically separated silicon islands insulated by a dielectrically separating oxide film on the wafer surface, the dielectrically separated wafer comprises a

surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat.

6. A dielectrically separated silicon wafer according to Claim 1 for which the flatness of the surface between these dielectrically separated silicon islands is less than 0.2 μm as the absolute value, which is the difference between the maximum value and the minimum value when this surface is measured by a stylus-profilometer.

7. A fabrication method for a dielectrically separated wafer comprising the steps of:

forming dielectrically separating grooves by anisotropic etching on the silicon wafer surface;

coating a dielectrically separating insulating film on the surface of a silicon wafer including these dielectrically separating grooves;

depositing a polysilicon layer by the high temperature CVD method on this dielectrically separating insulating film, and providing a plurality of dielectrically separated silicon islands insulated by a dielectrically separating insulating film by separation polishing the silicon surface of the side of the silicon wafer opposite to the side on which the polysilicon layer is deposited; and

wherein depending on the corrosion resistance of this deposited polysilicon layer, the thickness of this dielectrically separating insulating film, the etching depth for forming these dielectrically separating grooves, and the distance between neighboring dielectrically separated silicon islands, the surface between one dielectrically separated silicon island and a neighboring dielectrically separated silicon island is flattened by changing the conditions of the separation polishing of the silicon surface.

8. A fabrication method for a dielectrically separated wafer according to Claim 3 in which the flatness of the surface between these dielectrically

separated silicon islands is less than 0.2 μm, which is the absolute value of the difference between the maximum value and the minimum value when this surface is measured by a stylus-profilometer.

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A27